CLAIMS

What is claimed is:

1. A memory controlling apparatus comprising:

a memory module;

an address line;

a data line;

a first transmitter which transmits an address of read data, or an address of write data along with the write data to the memory module via the address line; and

a second transmitter which transmits data read from the memory module via the data line.

2. The memory controlling apparatus according to claim 1, wherein the memory controlling apparatus receives a command from an upper module to read data from the memory module, or to write data to the memory module, and controls the accessing of the memory module according to the command.

3. The memory controlling apparatus according to claim 1, wherein the first transmitter's transmission of an address of read data, or an address of write data along with the write data to the memory module via the address line, and the second transmitter's transmission of data read from the memory module via the data line are performed contemporaneously without causing a data bottleneck.

4. The memory controlling apparatus according to claim 1, wherein the read data and the write data are transmitted at both up and down edges of a clock signal.

5. The memory controlling apparatus according to claim 4, wherein the memory module comprises DDR SDRAMs.

6. The memory controlling apparatus according to claim 2, wherein the second transmitter transmits data read from the memory module to the upper module via the data line.

7. The memory controlling apparatus of claim 1, wherein the first transmitter comprises an address queue which sequentially stores the address of the read data, or the address of the write data and the write data, and keeps the stored address and the stored data in a state ready to be transmitted to the memory module.

8. The memory controlling apparatus of claim 1, wherein the first transmitter comprises an address queue, wherein when writing the write data,

the memory controlling apparatus stores the address of the write data in the address queue,

then stores the write data in the address queue, and

then sequentially transmits the stored address and the stored data to the memory module via the address line.

9. The memory controlling apparatus of claim 8, wherein when writing the write data in a full-write manner, the write data is divided into bytes, and the bytes are sequentially transmitted from the address queue to the memory module at their corresponding addresses.

10. The memory controlling apparatus of claim 8, further comprising an upper module of the system, wherein when writing data in a partial-write manner, predetermined bytes of data, transmitted from the upper module and corresponding to specific locations, are stored in the address queue and are then transmitted to the memory module according to the addresses stored in the address queue.

11. The memory controlling apparatus of claim 1, wherein the second transmitter includes a data queue which sequentially receives and stores data read from the memory module and keeps the stored data in a state ready to be transmitted to the upper module of the system.

12. The memory controlling apparatus of claim 2, wherein:

the first transmitter includes an address queue which sequentially stores the address of the read data, or the write data and the write data, and keeps the stored address and the stored data in a state ready to be transmitted to the memory module, and

the second transmitter includes;

a write data queue which sequentially receives data from the upper module of the system, stores the received data, and keeps the stored data in a state ready to be transmitted to the memory module via the address line, and

a read data queue which sequentially stores read data received from the memory module via a data line and transmits the stored read data to the upper module.

13. The memory controlling apparatus of claim 12, wherein when writing data, addresses stored in the address queue are transmitted to the memory module via the address line, and then data stored in the write data queue is transmitted to the memory module via the address line.

14. The memory controlling apparatus of claim 13, wherein when writing data in a full-write manner, the write data is divided into bytes and the bytes are then sequentially transmitted from the address queue to the memory module at their corresponding addresses.

15. The memory controlling apparatus of claim 13, wherein when writing the write data in a partial-write manner, predetermined bytes of data, that correspond to specific locations, are;

transmitted from the upper module,

stored in the address queue, and

then transmitted to the memory module according to corresponding addresses that have been stored in the address queue.

16. A memory controlling apparatus which receives, from an upper module of a system, a command to read data from a memory module or to write data in the memory module, and controls accessing the memory module in response to the command, the memory controlling apparatus comprising:

an address line;

a data line;

an address latch which latches address data;

a data latch which latches read data or write data;

an address and write data queue which;

sequentially stores,

an address, input from the address latch, and

the write data, from the data latch, and

transmits the stored address and the stored data to the memory module via the address line; and

a data queue which sequentially stores the read data, input from the memory module via the data line, and transmits the read data to the upper module.

17. A memory controlling apparatus which receives, from an upper module of a system, a command to read data from a memory module or to write data in the memory module, and controls accessing the memory module in response to the command, the memory controlling apparatus comprising:

an address line;

a data line;

an address latch which latches address data;

a data latch which latches read data or write data;

an address queue which stores an address input from the address latch and transmits the stored address to the memory module via the address line;

a write data queue which stores the write data input from the data latch and sequentially transmits the stored write data to the memory module via the address line; and

a read data queue which sequentially stores the read data input from the memory module via the data line and transmits the read data to the upper module.

18. A memory controlling apparatus comprising:

an address line;

a data line;

a memory;

a memory controller which transmits an address and write data via the address line and receives read data via the data line; and

a memory module comprising:

a memory buffer; and

a write data buffer;

wherein the memory module:

separates an address from the write data;

transmits the address and the write data to the memory buffer and the write data buffer, respectively;

writes the data on a memory cell indicated by the address; and

transmits data read from the memory to the memory controller via the data line.

19. The memory controlling apparatus according to claim 18, further comprising an upper module, wherein the memory controlling apparatus receives a command from the upper module to read the read data from the memory module, or to write the write data to the memory module, and controls the accessing of the memory module according to the command.

20. The memory controlling apparatus of claim 19, wherein the memory controller comprises:

a memory module;

an address latch which latches address data;

a data latch which latches the read data or the write data;

an address and write data queue which sequentially stores an address input from the address latch and the write data from the data latch and transmits the stored address and the stored data to the memory module via the address line; and

a data queue which sequentially stores the read data input from the memory module via the data line and transmits the read data to the upper module.

21. The memory controlling apparatus of claim 20, wherein when writing the write data in a full-write manner, the write data is divided into bytes and the bytes are sequentially transmitted from the address queue to the memory module at their corresponding addresses.

22. The memory controlling apparatus of claim 20, wherein when writing the write data in a partial-write manner, predetermined bytes of data that correspond to specific locations are:

transmitted from the upper module of the system; stored in the address queue; and

transmitted to the memory module along with corresponding addresses stored in the address queue.

23. The memory controlling apparatus of claim 18, wherein the memory controller comprises:

an address latch which latches address data;

a data latch which latches the read data or the write data;

an address queue which stores an address input from the address latch and transmits the stored address to a memory module via an address line;

a write data queue which stores the write data input from the data latch and sequentially transmits the stored write data to the memory module via the address line; and

a read data queue which sequentially stores the read data input from the memory module via a data line and transmits the read data to the upper module.

24. The memory controlling apparatus of claim 23, wherein when writing data in a full-write manner, the write data is divided into bytes and the bytes are sequentially transmitted from the address queue to the memory module at their corresponding addresses.

25. The memory controlling apparatus of claim 23, wherein when writing the write data in a partial-write manner, predetermined bytes of data that correspond to specific locations are transmitted from the upper module of the system, the bytes of data are then stored in the address queue, before being transmitted to the memory module with their corresponding addresses stored in the address queue.

26. The memory control apparatus of claim 18, wherein the memory module further comprises:

a column address buffer which stores column addresses included in address data received via the address line;

a row address buffer which stores only row addresses included in the address data;

a write data buffer which stores data received via the address line;

a memory cell where data stored in the written data buffer is written on a predetermined place indicated by a column address and a row address received from the column address buffer and the row address buffer, respectively, in a data write mode and is read from the corresponding address in a data read mode; and

a read data buffer which stores the data read from the memory cell and transmits the stored data to the memory controller.

27. A memory controlling apparatus comprising:

a memory module;

a memory controller;

a first transmission line, which transmits only column address, row address, and/or write data from the memory controller to the memory module; and

a second transmission line, which transmits only read data from the memory module to the memory controller.

28. A memory controlling apparatus which receives, from an upper module of a system, a command to read data from a memory module or to write data in the memory module, and controls accessing the memory module in response to the command, the memory controlling apparatus comprising:

an address line, which transmits only column address, row address, and/or write data to the memory module; and

a data line, which transmits only read data from the memory module.